EE/CprE 4920 – sdmay25-26
Status Report 1
12/16/2024 - 1/30/2025

Cost-Effective and Easily Configurable High Voltage Motor Controllers for Automotive Use

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Summary

Software development is moving along and nearing a state where it can undergo tests and, eventually, a full integration test. The MCU pinout and hardware schematic are finalized. The PCB and all the components will be ordered soon. The regular advisor meeting for this semester is still to be determined.

Accomplishments

Developed both the logic board and power board, revised based on feedback, and are set to order parts. Software is almost done with what is needed for basic motor tests to be run when boards are assembled, and low-level drivers are being developed for SAMC21J18.

Pending Issues

None at the moment.

Individual Contributions

Member	Contributions	Period Hours	Cumulative Hours
Gavin Patel	Developed low level abstractions for SAMC	5	60
Bryce Rega	Developed PID and motor timing software	8	71
Marek Jablonski	Designed Logic Board Schematic and PCB	13	78
Jonah Frosch	Redesigned the Gate Driver board	20	79
Long Yu	General part organization	4	56

Plans for next reporting period

Hardware:

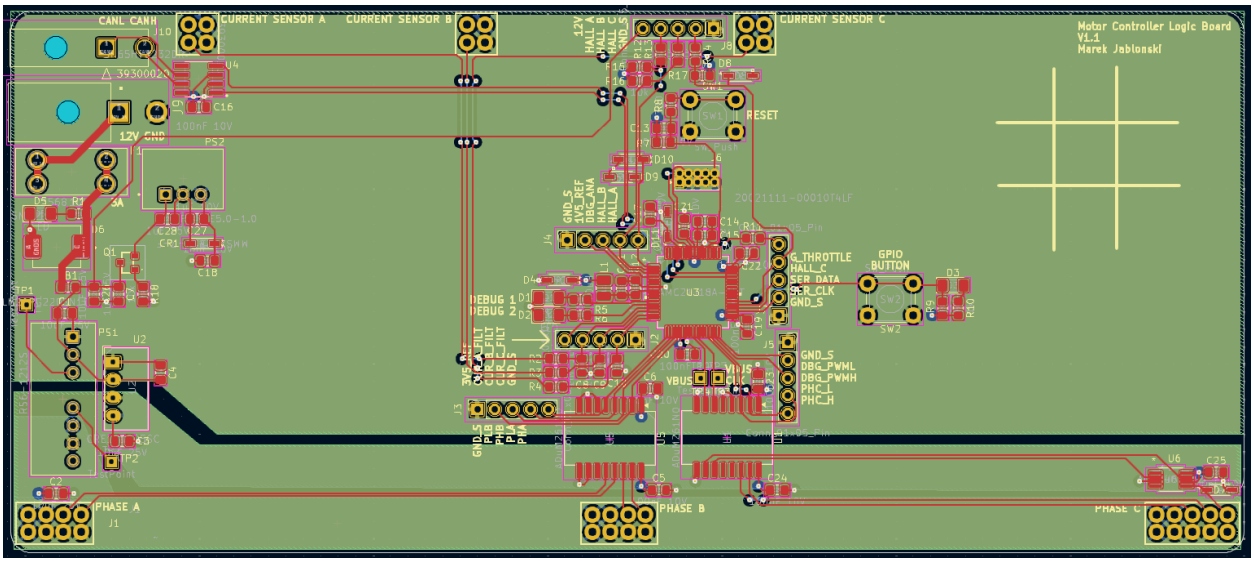
PCBs and BOM components will be ordered. If they arrive before the end of the next period they will be assembled. High Voltage Capacitors will be tested and characterized for capacitance across voltage and voltage tolerance.

Software:

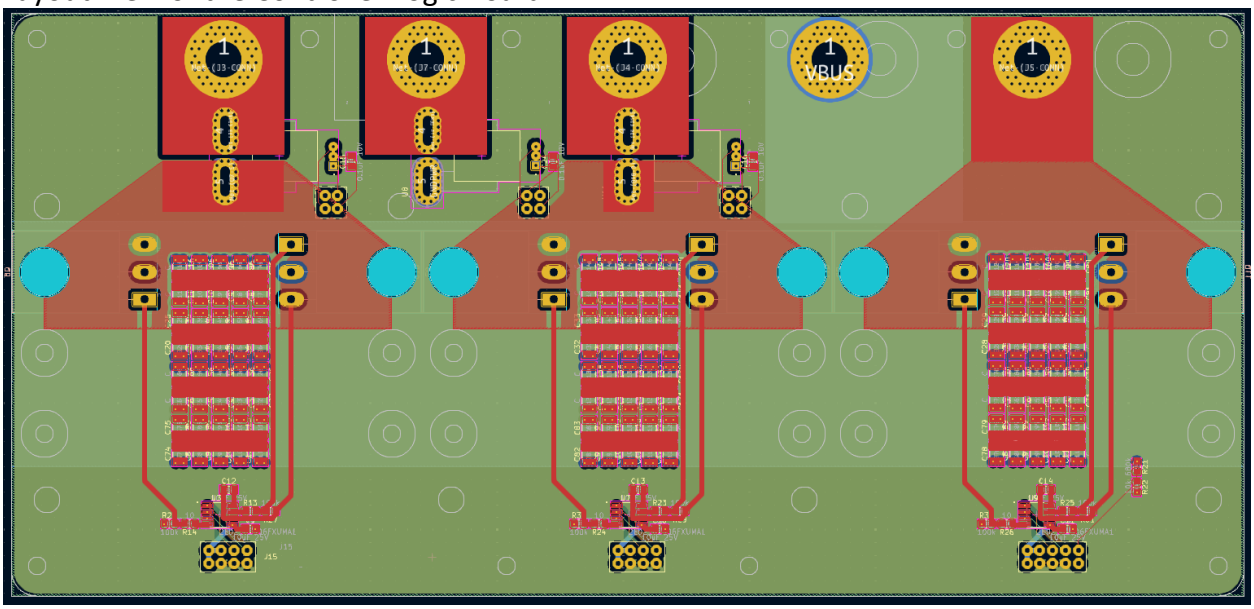
Need to have basic motor tests ready by the time the board gets here.
Continuing developing low level drivers and continue basic motor development.

Project Work

Hardware:



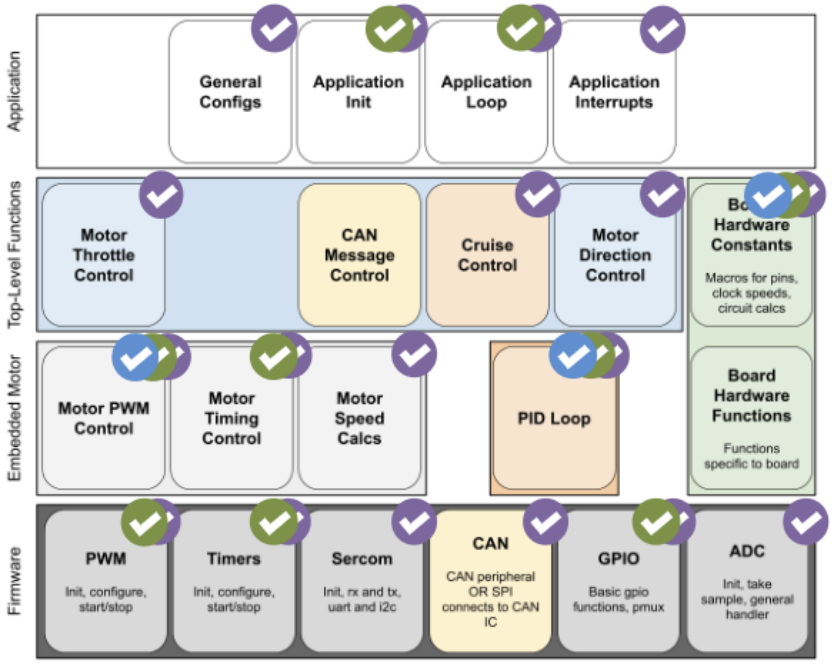
Layout View of the Controller Logic Board.



Layout View of the Controller Power Board

Software:
GPIO low level drivers made for SAMC chip.
PIC controller finished for basic motor testing.

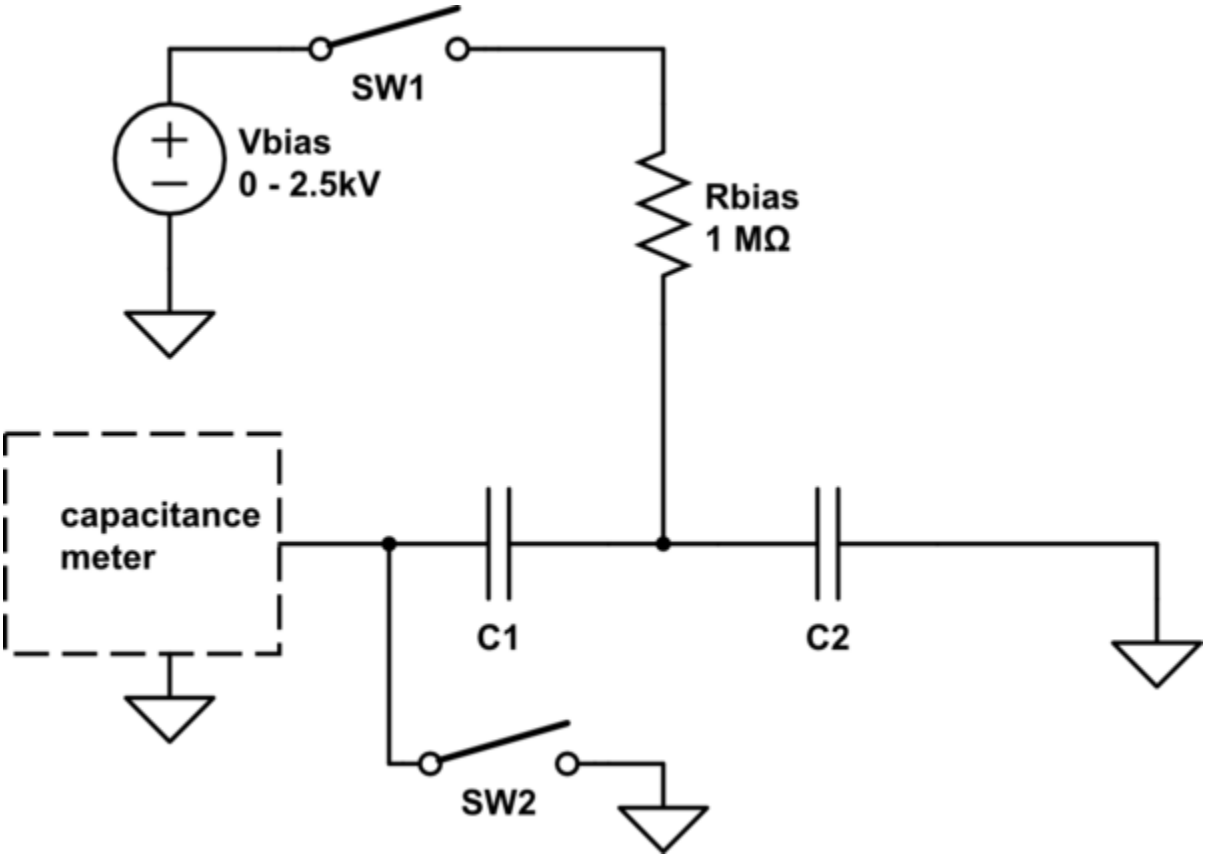
Software Progress Map



Purple indicates header files and plan is written. Green indicates skeleton code with documentation is generated. Blue indicates functionality (not tested, but potentially useable).

Initially, only the bottom and top layers had work, but now we are at the stage where the middle layers that are more complicated and go into the “unknown” a bit more are being worked on.

Research



Capacitor characterization schematic. C1 and C2 are the DUT.
Source: https://electronics.stackexchange.com/questions/729933/what-is-the-best-method-for-measuring-high-voltage-capacitor

Advisor Meeting Summary

We met with Professor Cheng Huang to discuss our final first prototype revision, where our MCU was broken out to a separate logic board daughterboard to a gate driver board. Save for comments on adding space for an optional electrolytic capacitor and some inductance concerns from the drivers to the power FETs, the boards appeared to be good enough to go ahead and order for a revision 1.